Journal of Applied Science, Engineering, Technology, and Education *ISSN: 2685-0591 (online)*
Vol. 5 No. 1 (2023)
https://doi.org/10.35877/454RI.asci1649

High Speed and Low Leakage Power Voltage Level Shifter using Regulated Cross-Coupled Network

Mohan Rao Thokala

Department of Electronics and Communication Engineering, National Institute of Technology Calicut, Kerala State, India

Abstract

This concise presents a power efficient level shifter using regulated cross-coupled network with split inverter. With the use of regulated cross-coupled network, power dissipation of the pull-up region drastically decreases. Level shifters convert the voltage levels which are below the threshold voltage to the acceptable voltage levels by decreasing the transistor size. A Split inverter is used at the output to decrease the short circuit current. Modified Split inverter along with the load capacitor at the output is used to increase the speed and to decrease the power consumption. This LS can save 31% power compared to other techniques. The proposed level shifter works effectively at high speed and consumes less power. For simulation, LT spice tool of 50 nm technology and 90 nm technology is used.

Keywords: Level shifter, split-inverter, RCC network, threshold level, leakage power, short-circuit power.

Received: 22 February 2023 Revised: 19 May 2023 Accepted: 2 June 2023

1. Introduction

Level shifter is a circuit, that is used to convert signals from one logic state to another logic state, which is applicable to circuits like CMOS and TTL. Level shifters are used in various domains like processor applications, sensors and VLSI design circuits. Voltages of 3.3V ,1.8V and even less voltage values are needed. Digital systems use level shifters to provide different voltage level logics to different blocks of a system, without shifters it is difficult to provide different voltages to different blocks within the system. Transition from high to low is often optional, but conversion from low to high is required in most cases. Level shifters are placed at the top, bottom or can be even at midway of circuit.

Power dissipation depends on supply voltage, load capacitance, frequency and on switching activation factor. By decreasing all these, we can reduce the power dissipation. Reducing the supply voltage by half decreases the power dissipation to 75%, but it affects the performance. For CMOS transistor, both static power and dynamic power are present. Leakage power occurs when the circuit is in the OFF state. Short circuit power and switching power both will play a key role in dynamic power dissipation; the dynamic power is present when circuit is switching (Luo, Huang, & Chu, 2014). There are many techniques to reduce the dynamic power by transistor sizing, clock gating, power gating, logic optimization, multiple supply voltage, pipeline, parallel processing, architecture planning, etc. In all the cases, by bringing down the supply voltage, the power dissipation reduced greatly, but it costs the speed performance. By providing different voltages to different blocks using a level shifter is a good choice (Maghsoudloo, ezaei, Sawan, & Gosselin, 2016; Hosseini, Saberi, & Lotfi, 2017). Supply voltages for the MOS transistors which are less than its Vth, possible with level shifters. Level shifter using a cross-coupled network drastically reduces the power dissipation and the speed of getting output increases. This LS method is usable for a large range of inputs.

* Corresponding author.
E-mail address: mohan_p220124ec@nitc.ac.in

2. Literature Survey

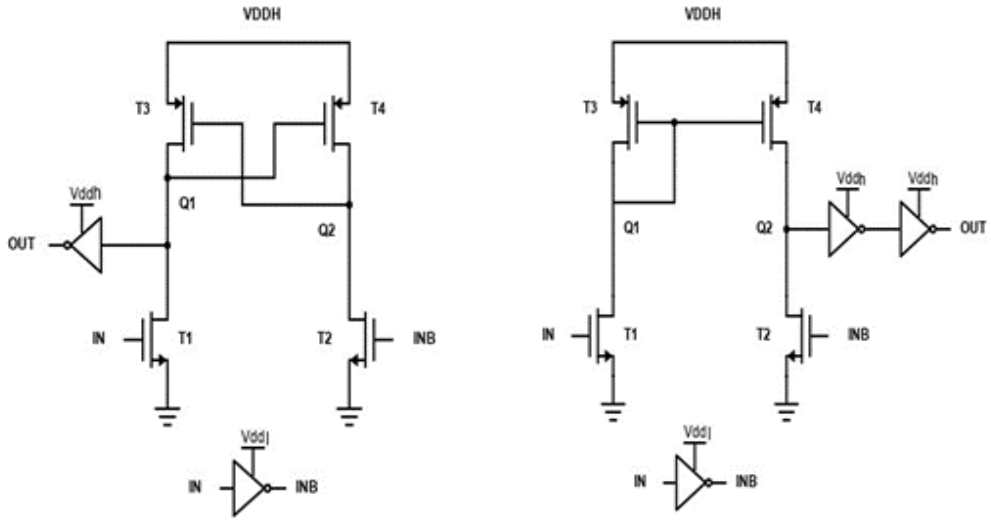
2.1. Level Shifters

2.1.1. LS using Current Mirror

Level shifters can be implemented using current mirror, but there is one disadvantage with this design is that, there is no proper interaction between the pull-down transistors and pull-up transistors, it causes to high standby power is present due to static current.

2.1.2. LS using DCVS

DCVS based LS consists of cross-coupled network at pull-up, it can improve the interaction between pull-up and pull-down transistors which can cause to increase the speed. Standby power decreases as no static current exists, but pull-down transistor decreases when VDDH is less than Vth because NMOS transistor won't go beyond PMOS transistor. To increase the strength of transistors, the size of the transistors is scaled which in turn decreases the efficiency of the circuit (Hosseini, Saberi, & Lotfi, 2017).



(a) LS using DVCS (b) LS using Current Mirror

Figure 1. LS using DVCS and Current Mirror

2.1.3. LS by using modified Wilson current mirror

LS using Wilson current mirror helps to maintain proper rise time and fall time but when VDDH and VDDL values are close to each other, the delay increases due to lack of driving. OR gate and delay path is introduced in order to increase the driving strength, as well as to control the leakage current (Luo, Huang, & Chu, 2014).

2.1.4. LS using feedback path

Self-controlled circuity is possible by providing the feedback path from the output to the input. It can convert the sub-threshold voltage to the voltage level above threshold level, ration of pull-up transistor is less compared to pull-down transistor so that pull-down transistor capacity will decrease, which causes to increases the short-circuit current. To reduce the short-circuit current, pull-up transistor is built with a low threshold transistor and pull-down transistor with a high threshold transistor (Alioto, 2012; Lanuzza et.al., 2017).

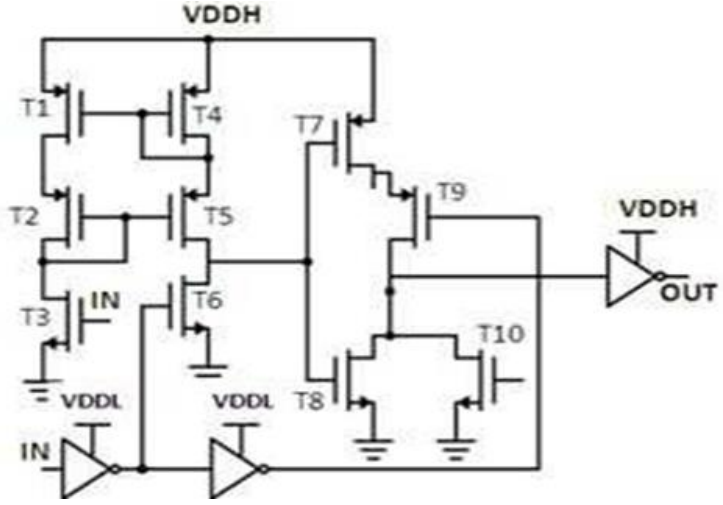


Figure 2. LS with Modified Wilson Current Mirror

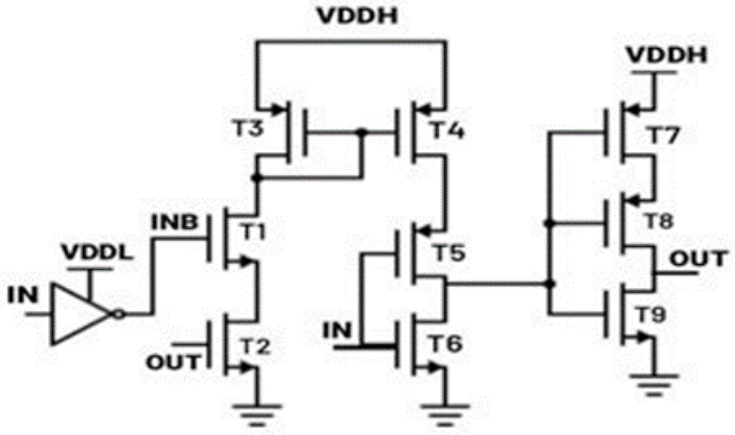


Figure 3. LS with Feedback Path

2.2. Existing Method

Existing LS uses DCVS structure which consists of RCC pull up network to increase the strength of pull up network and to increase the efficiency of charging and discharging at internal nodes, this will increase the switching speed. The circuit consists split inverter, current limiters and RCC network. The spilt inverter at the output is placed to reduce the short leakage current from pull-up transistors. The main advantage of shifter is, PMOS transistors will never be switched-off when they have gone to the sub-threshold region, with this we can get quick response and contention current can be minimized. A Current limiter is used to reduce the contention current. To increase the conversion, the size of pull-down transistors increased with this we can convert very low voltage to high level using this LS. T5 and T6 transistors are used to decrease the strength of pull-down transistors.

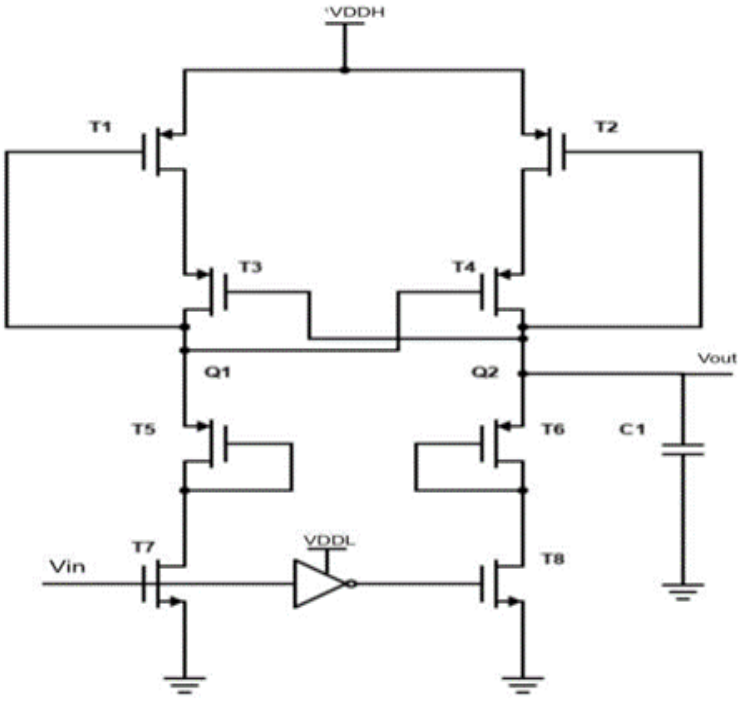


Figure 4. LS with RCC Network

2.3. Proposed Method

Transistor current is decreased in the pull-up region and increased in the pull-down region with auxiliary by modifying the transistor size, with the result we can decrease the delay. A split inverter is used at the output to decrease the short circuit current.

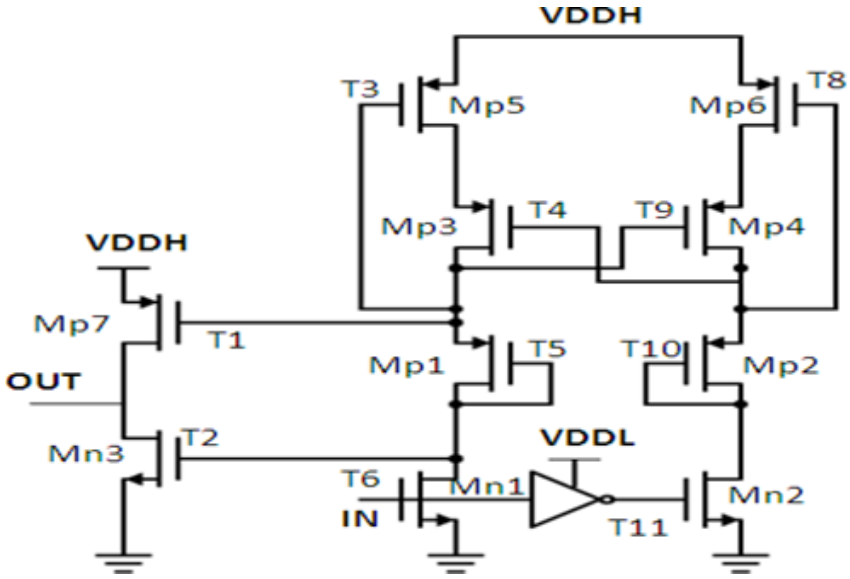


Figure 5. LS with Output Split Inverter

LS is used to convert the sub-threshold voltage levels which are below the threshold voltage to acceptable voltage levels. A split inverter is used to decrease the short circuit current. In this modified circuit, leakage power is decreased by SAPON technique in which PMOS and NMOS transistors (Q3&Q4) remain in active, irrespective of the input transition. SAPON (Stackly Arranged Low Power ON Transistor) technique is used to reduce the leakage power. Total power in the transistor includes static power and dynamic power. Mostly static power consists of leakage power and dynamic power includes, both switching power and short circuit power (Lorenzo & Chaudhury, 2017; Hanchate & Ranganathan, 2004)).

2.3.1. Static leakage power

Leakage power is occurred due to the P-N junction reverse biased current. Sub-threshold current generated for short channel devices below threshold voltages. Sub-threshold depends on thermal voltage, actual gate voltage and threshold voltage difference.

Reverse biased current is given by

$$I_D=I_S\ (e^{V/Vt}-1)$$

& sub-threshold current is given by

$$I_{SUB} = I_O e^{\frac{V_{GS}-V_{THO}-\eta V_{DS}+\gamma V_{BS}}{nV_T}}\left(1-e^{\frac{-V_{DS}}{V_T}}\right)$$

2.3.2. Short circuit Leakage power

Short circuit power plays a key role in dynamic power consumption. Due to fall time and rise time of transistors, there exist short-circuit path between VDD to ground and leads to power dissipation.

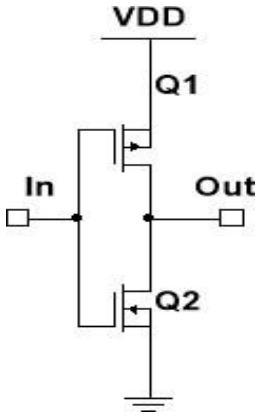


Figure 6. Existing Inverter

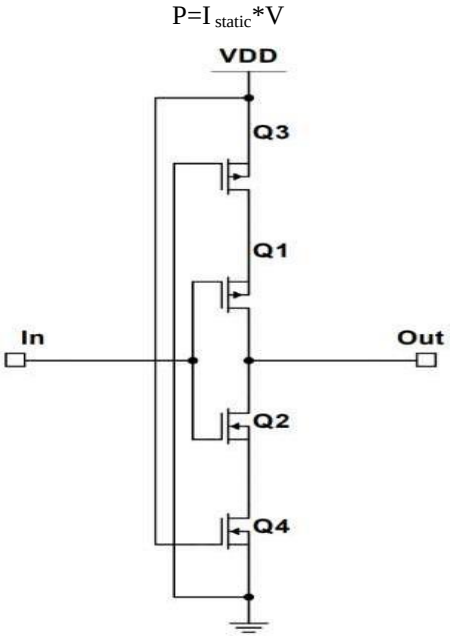


Figure 7. Proposed SAPON based Inverter

When logic 0 is given to the inverter. PMOS pull-up transistor will turn ON and NMOS pull-down transistor is switched-OFF and SAPON transistors (Q3 and Q4) remain in the active region, output reads logic 1 (Abdollahi, Fallah, & Pedram, 2004). Similarly, when logic 0 is given as input to the inverter, PMOS transistor will be turned off and NMOS transistor turned on and the output gets pulled down to 0[10'12]. It reduces the leakage power, power can be saved 31% compared to other techniques i.e., LECTOR (6%), LCNT (3%), STACK ONOFIC (11%).

Table 1. SAPON Inviter transition

Input	PMOS	NMOS	SAPON	
			Transistors	Outpur
0	ON	OFF	ON	1
1	**OFF**	**ON**	**ON**	**0**

3. Implementation of LS with Sapon Split Inverter

LS with split inverter is used at the output and this split inverter is implemented with SAPON technique is used to reduce both leakage power and short-circuit power. Figure 8 shows transistor condition during input transition from 0 to 1, and figure 9 shows for 1 to 0 transition.

During input transition from 1 to 0, N1 node is at HIGH and value N2 node is at low, it will switch on T2, T3 and T1, T4 will be OFF. When input transition 0 to 1 T7 will be ON and T8 will be OFF. It will pull the value N1 to low and when it is discharging, T1, T4 will switch ON and T2, T3 are switched OFF. At this instant, the N2 node will start charging, as the output is connected to N2 through the capacitor.

The capacitor will charge to the value of N2. Here PMOS transistors will go to the sub-threshold region but will never be switched off because the get input value of VDDH-Vth. Pull up transistors will never go to switched-OFF, causes to speed of response is increased. When input transition at input, the same process is repeated but in inverse N1 node to be HIGH and N1 node will be at LOW.

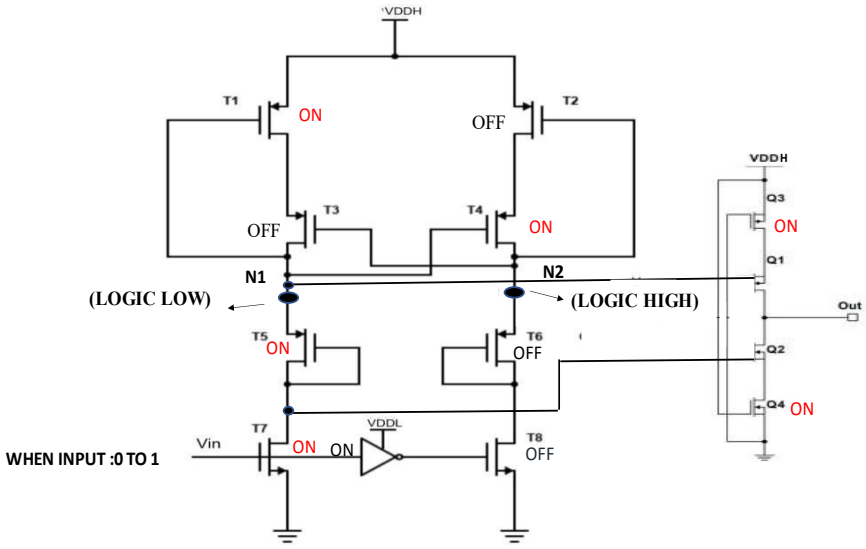


Figure 8. LS using RCC network and SAPON for Input Transition from 0 To 1

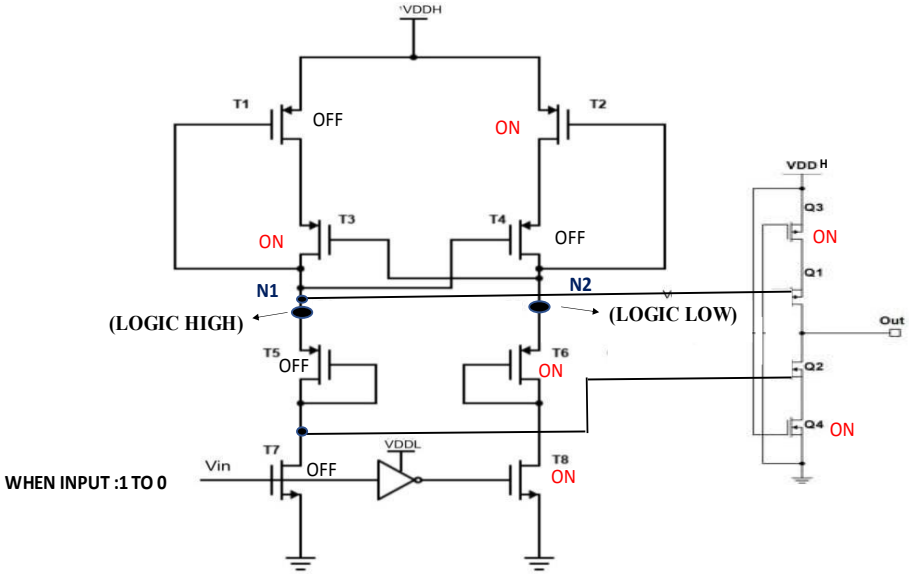


Figure 9. LS using RCC network and SAPON for Input transition from 1 To 0

4. Simulation Results

Figure10 displays the schematic of LS with RCC& SAPON inverter using 50nm technology, Input pulse is given with rise time & fall time taken as ‘0’, initial voltage is taken as ‘0’, Von voltage taken as ‘0.25’ volts, Ton time is’10m’ time period is ‘20ms’, number of cycles ‘5’. W/L ratio of PMOS transistors M1, M2, M3, M4, M5, M6, M10, M12, M13 is 0.4um/50nm and NMOS transistors as M7, M8, M9, M11, M14 is 0.2um/50nm.it can sub-threshold region of 0V to 0.5V with power dissipation of 88nw and leakage current of 246µA.

Figure 11 displays the simulation results of LS with RCC & SAPON inverter using 90nm technology, pulse input is given with rise time & fall time taken as '0', initial voltage is taken as '0', Von voltage taken as '0.45' volts, Ton time is 10m, time period is '40ms', number of cycles '30'. W/L ratio of PMOS transistors M1, M2, M3, M4, M5, M6, M10, M12, M13 is 0.4um/90nm and NMOS transistors as M7, M8, M9, M11, M14 is 0.2um/90nm.it can sub-threshold region of 0V to 0.9V with power dissipation of 72nW and leakage current of 129µA.

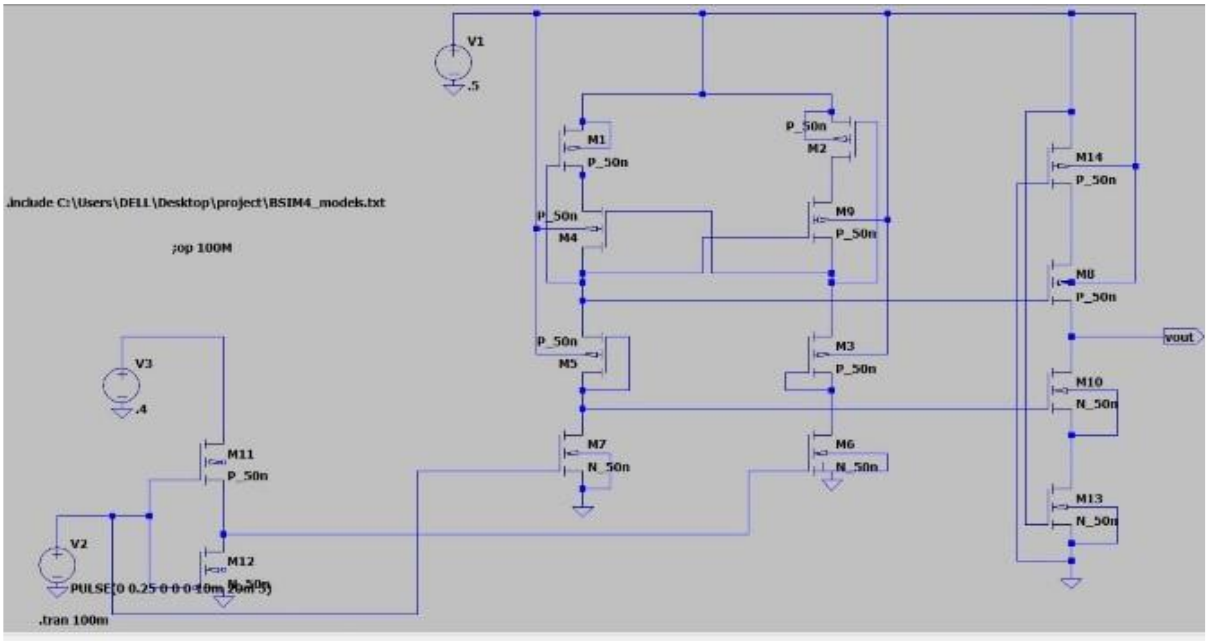


Figure 10. 50 nm technology based Schematic Diagram of LS using SAPON Inverter

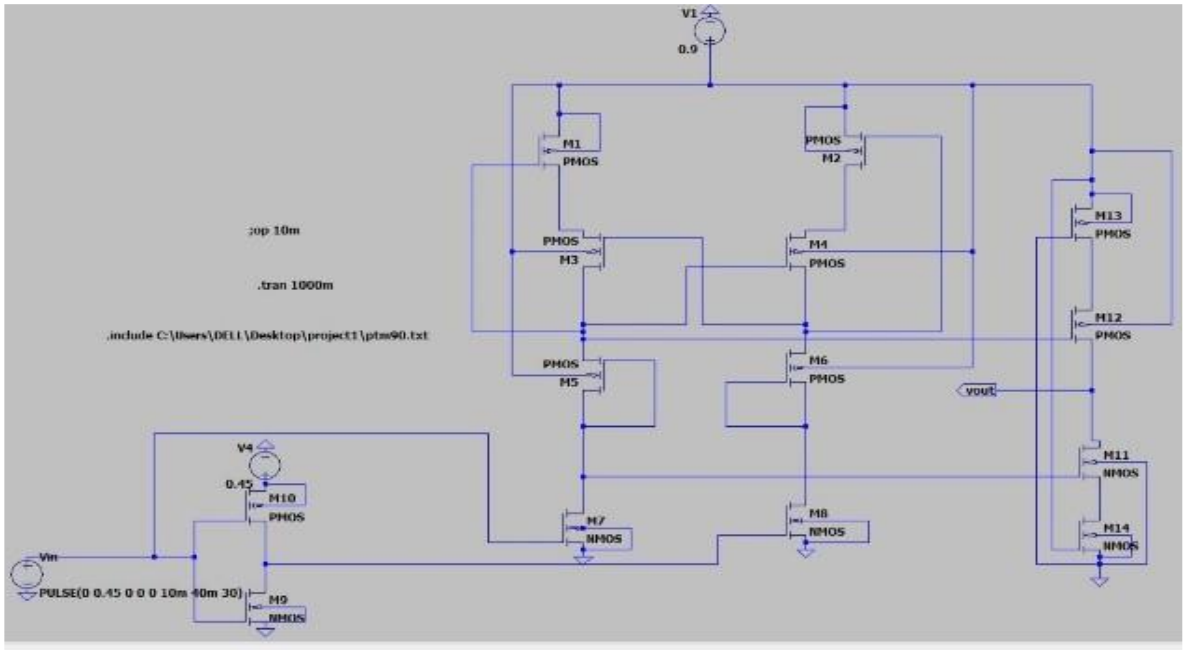


Figure 11. 90 nm technology based Schematic Diagram of LS using SAPON Inverter

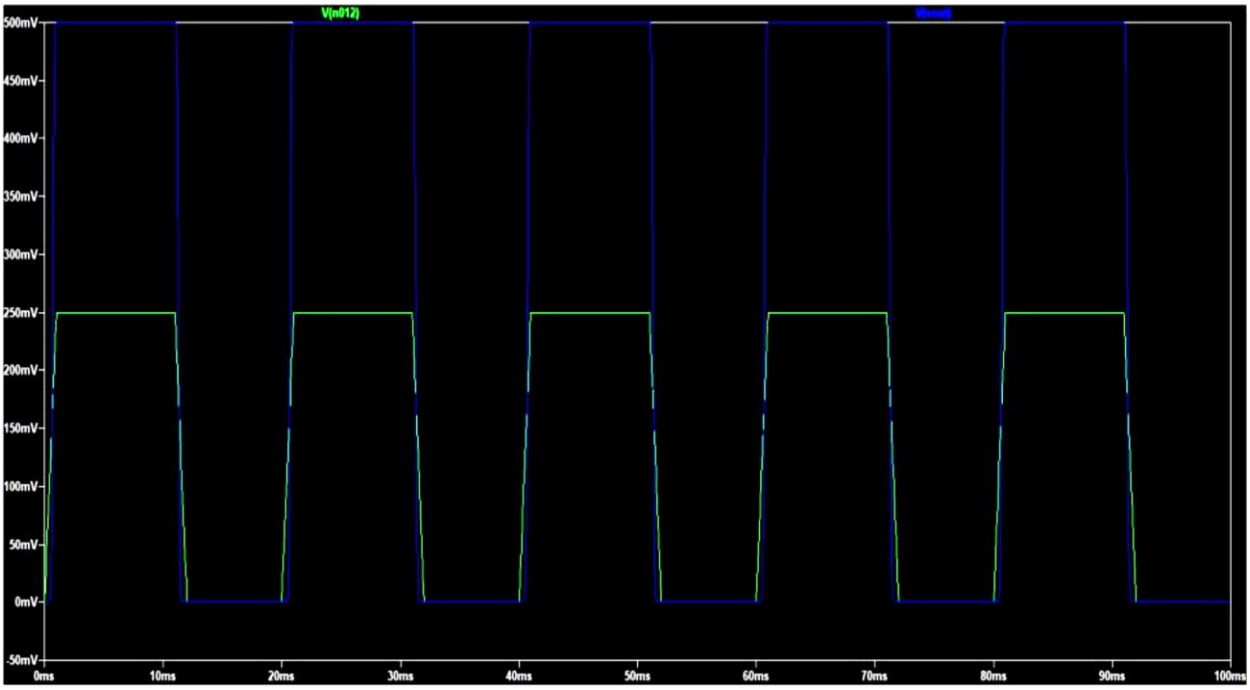


Figure 12. Simulation Results of 50nm Technology

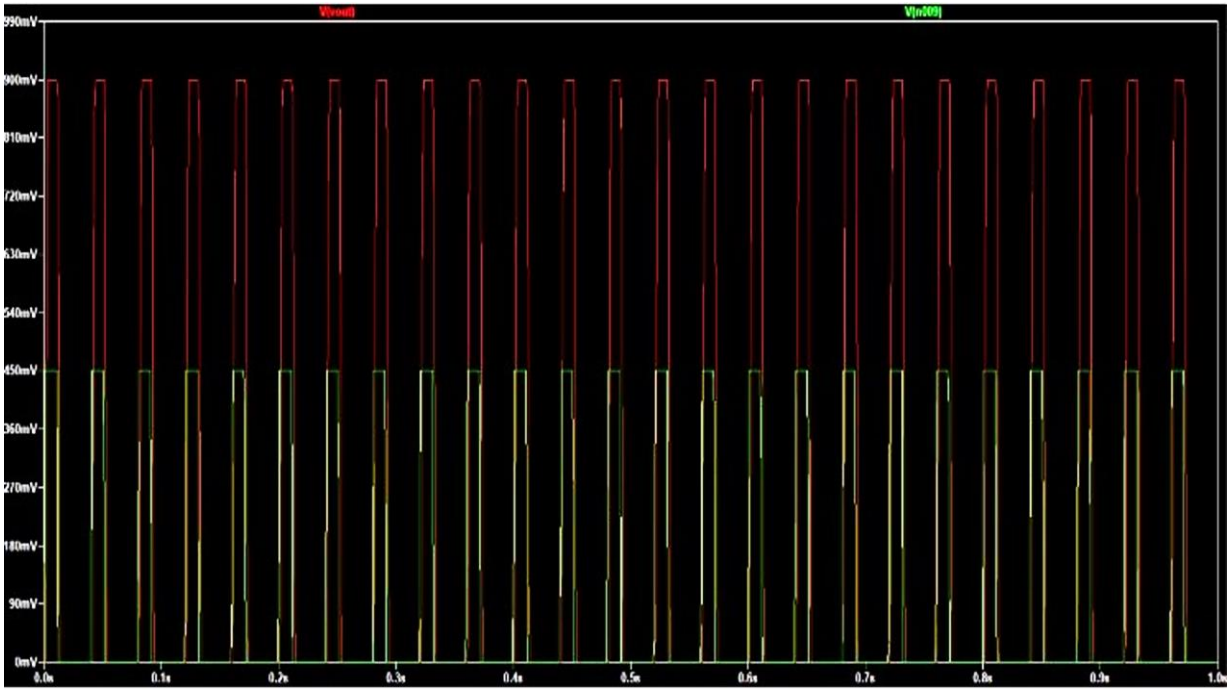


Figure 13. Simulation results of 90nm Technology

5. Conclusion

Proposed circuit decreases the leakage power dissipation, increases the speed by regulated cross-coupled network & current mirror connection. Leakage power can be decreased by SAPON technique without area overhead. At the output split inverter is used to reduce the short circuit current and this split inverter is implemented with SAPON technique which can reduce both static leakage power and dynamic short circuit power. It can convert the sub-threshold region 0V to 0.5V using 50 nm technology and 0V TO 0.9V using 90nm technology. Leakage power is decreased 32% compared to existing LS.

References

Abdollahi, A., Fallah, F., & Pedram, M. (2004). Leakage current reduction in CMOS VLSI circuits by input vector control. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *12*(2), 140-154.

Alioto, M. (2012). Ultra-low power VLSI circuit design demystified and explained: A tutorial. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *59*(1), 3-29.

Hanchate, N., & Ranganathan, N. (2004). LECTOR: a technique for leakage reduction in CMOS circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *12*(2), 196-205.

Hosseini, S. R., Saberi, M., & Lotfi, R. (2017). A high-speed and power-efficient voltage level shifter for dual-supply applications. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *25*(3), 1154-1158.

Lanuzza, M., Crupi, F., Rao, S., De Rose, R., Strangio, S., & Iannaccone, G. (2017). An ultralow-voltage energy-efficient level shifter. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *64*(1), 61-65.

Lorenzo, R., & Chaudhury, S. (2017). LCNT-an approach to minimize leakage power in CMOS integrated circuits. *Microsystem Technologies*, *23*, 4245-4253.

Luo, S. C., Huang, C. J., & Chu, Y. H. (2014). A wide-range level shifter using a modified Wilson current mirror hybrid buffer. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *61*(6), 1656-1665.

Maghsoudloo, E., Rezaei, M., Sawan, M., & Gosselin, B. (2016). A high-speed and ultra low-power subthreshold signal level shifter. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *64*(5), 1164-1172.

Usami, K., Igarashi, M., Minami, F., Ishikawa, T., Kanzawa, M., Ichida, M., & Nogami, K. (1998). Automated low-power technique exploiting multiple supply voltages applied to a media processor. *IEEE Journal of Solid-State Circuits*, *33*(3), 463-472.